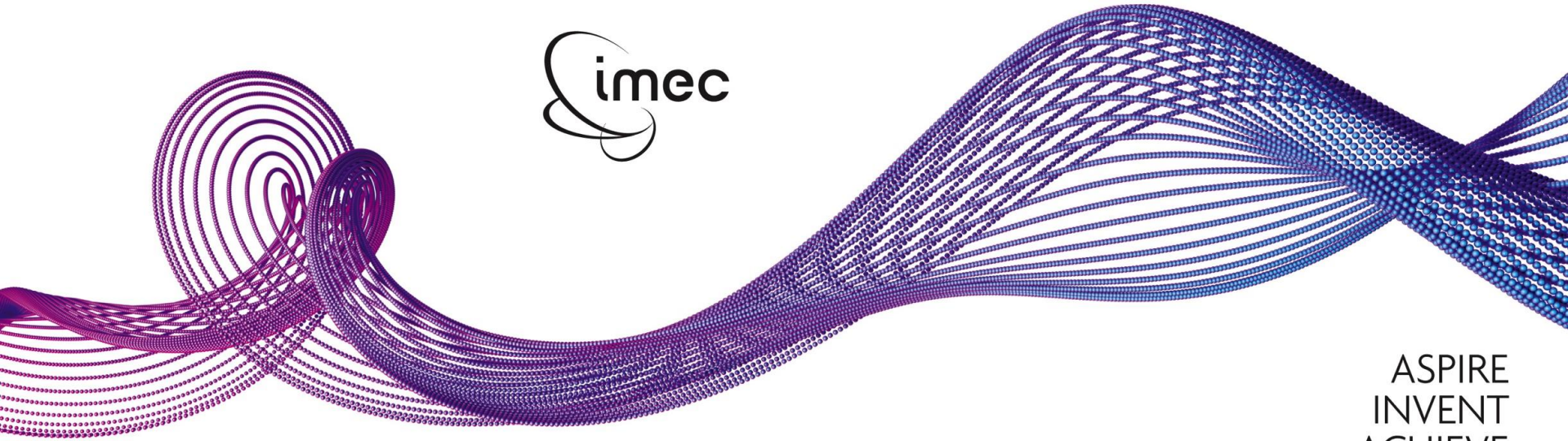
RECONFIGURABLE GLOBAL NEUROMORPHIC SYNAPSE INTERCONNECTS WITH TFTS

JAN GENOE, PRAVEEN RAGHAVAN, ZSOLT TOKEI, FRANCKY CATTHOOR, AND SOEREN STEUDEL



ASPIRE
INVENT
ACHIEVE

Every neuron in a human brain is connected via its synapses to 10-15.000 other neurons.

Those connections can be over time reconfigured allowing new connections with any other neuron. But only few of the longer connections are concurrently active

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GLOBAL SYNAPSE

In a neuromorphic IC with more then >1000 neurons, where every neuron can communicate with every neuron, the transistor count of the reconfigurable interconnect (switches, buffer, repeater) heavily dominates the transistor count, area and power consumption of the IC.

Objective

Large scale reconfigurable interconnect that allows to connect every neuron with every neuron even across the whole neuromorphic IC but with only limited amount of them concurrently active (as motivated earlier)

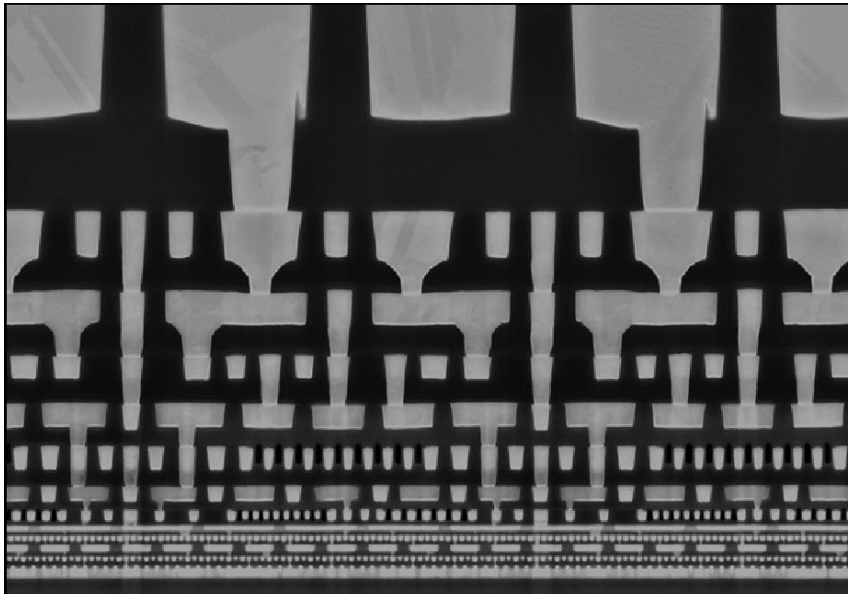
Scaling in power consumption
Scaling in integration density
Scaling in cost

BEOL OF N14 (INTEL)

Table 1. Pitch, thickness and metal aspect ratio for the BE stack. (ULK: Ultra Low k; LK: Low k)

Metal	Process	Dielectric	Pitch (nm)	Layer Thx (nm)	Metal Thx (nm)	AR Aspect ratio
0	PD SAV	LK CDO	56	70	40	1.4
1	PD SAV	ULK CDO	70	81	42	1.2
2	PD SAV	ULK CDO	52	73	40	1.5
3	PD SAV	ULK CDO	56	76	37	1.3
4	SAV	Air Gap	80	145	75	1.9
5	SAV	ULK CDO	100	210	110	2.2
6	SAV	Air Gap	160	310	180	2.3
7	SAV	ULK CDO	160	380	200	2.5
8	SAV	ULK CDO	160	400	200	2.5
9	Via First	LK CDO	252	540	260	2.1
10	Via First	LK CDO	252	675	375	3.0
11	Via First	SiO2	1080	1770	1080	2.0
12	Plate Up	polymer	14000	~	6000	1.3

Pitch / Metal Thickness



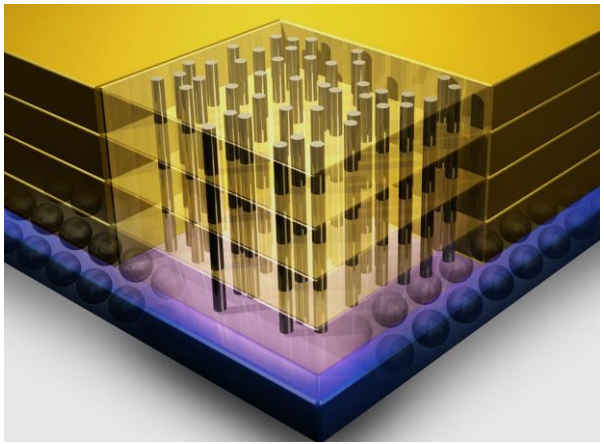
For the global interconnect (BEOL > M4) the via size dominates the area consumption of switches and repeaters. Not the FEOL transistor

K. Fischer et al, "Low-k interconnect stack with multi-layer air gap and tri-metal-insulator-metal capacitors for 14nm high volume manufacturing , Proceeding of IEEE MAM (2015)

3D INTEGRATION

3D TSV chip stacking

Stacking multiple identical chips with TSV

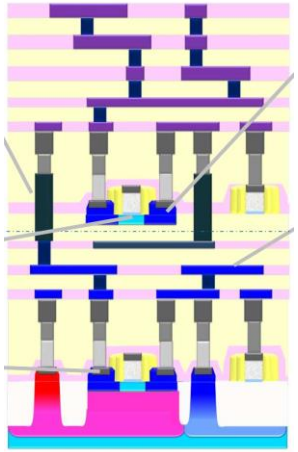


Pro:
High speed, high performance, relative mature

Con:
High cost,
integration density/size of TSV?

Monolithic 3D

Transfer of crystalline Si

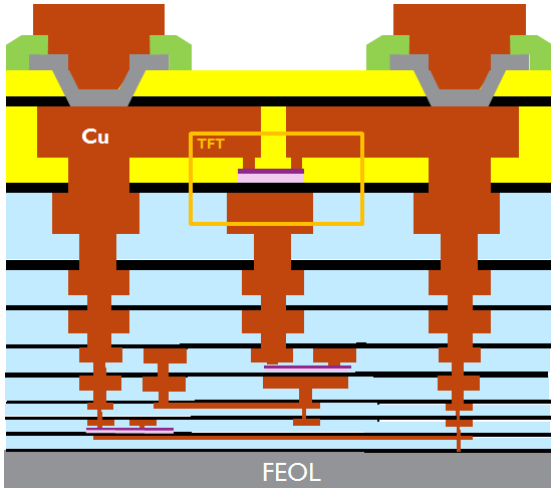


Pro:
high performance, high speed

Con:
Integration density? since only few (2) transistor layer are stacked

3D BEOL TFT

Integrate thin film transistors in the BEOL

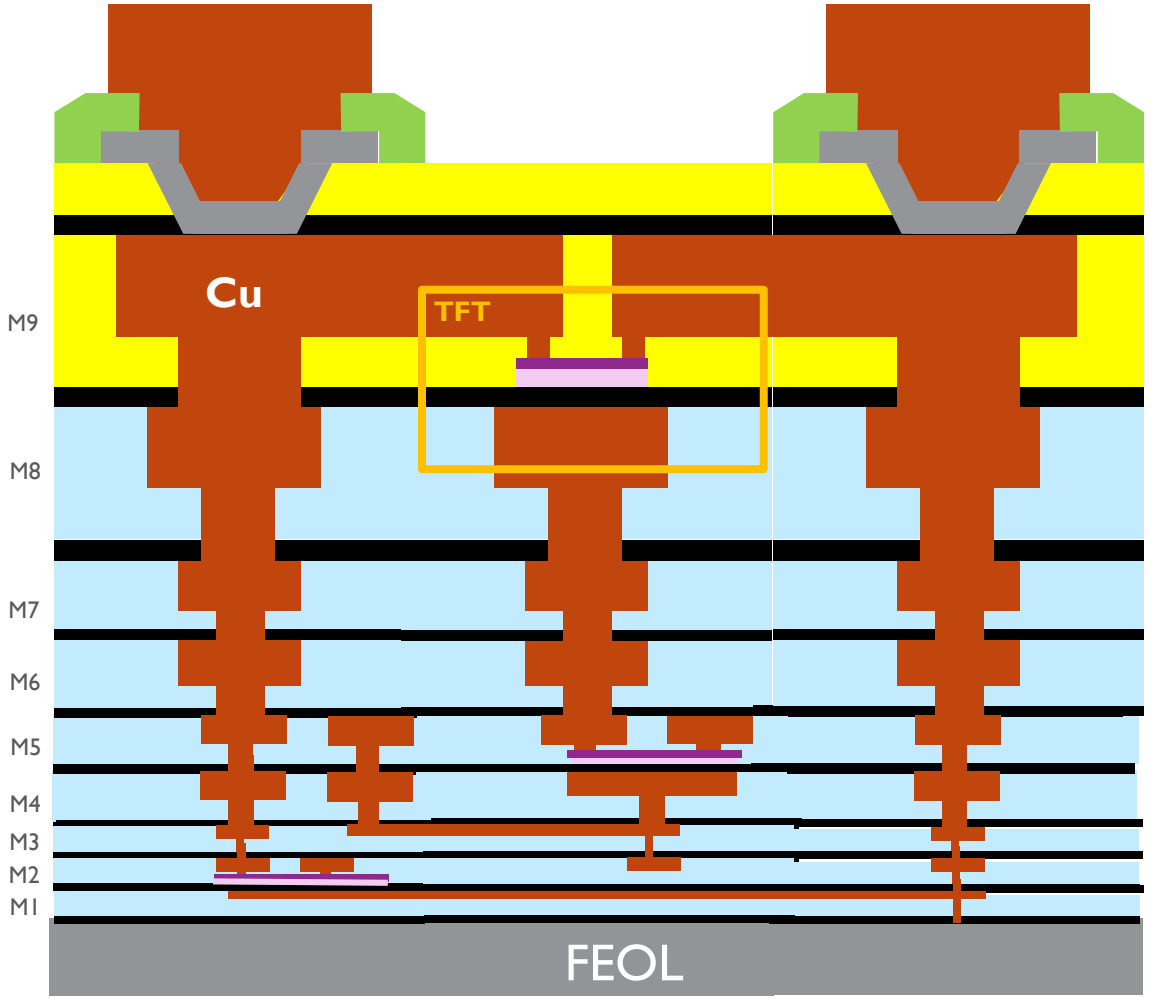


Pro:
Low cost?, high integration density

Con:
Performance, maturity

3D BEOL TFT

Enable in every BEOL layer a TFT process module with minimal additional mask count (cost) and a critical dimension that corresponds to the existing pitch of the metalization

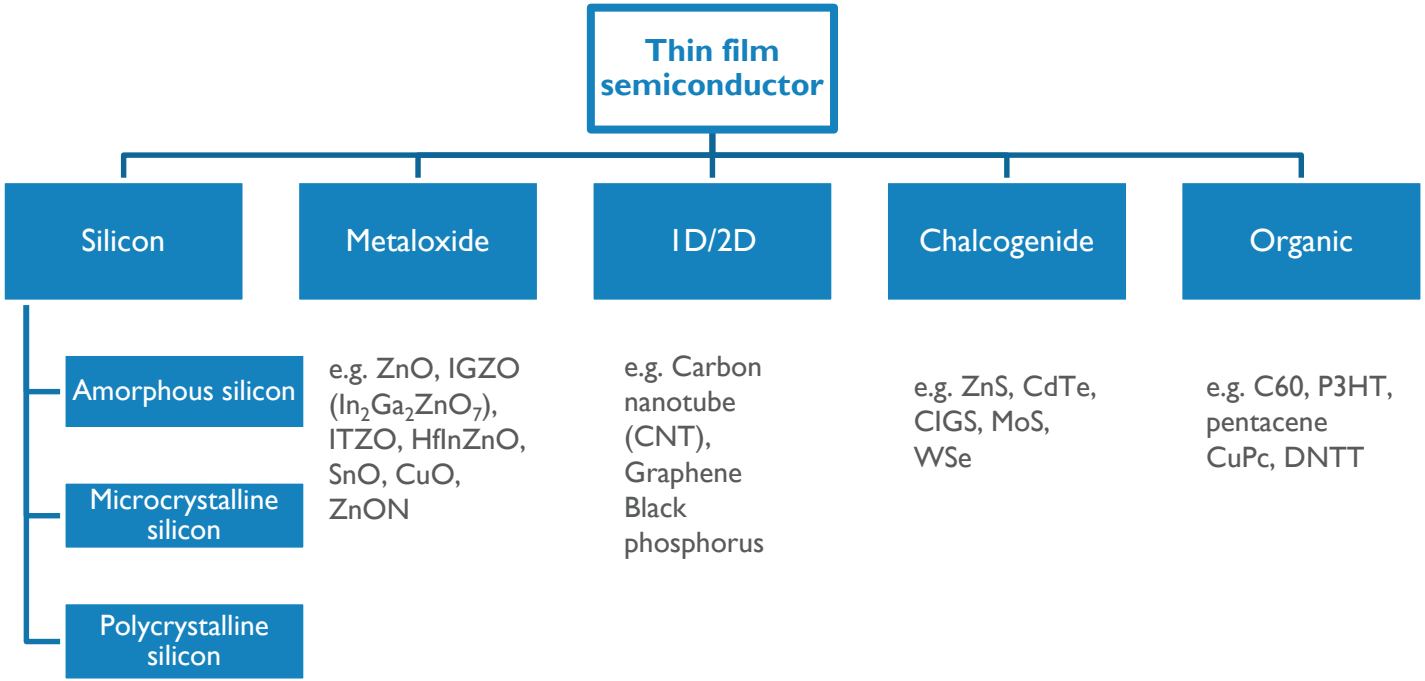


3D BEOL TFT

TFT REQUIREMENTS

1. **Scalability** down to pitch of M3-M4 (L<50nm)
2. **Temperature** budget of BEOL (380°C)
3. **Leakage** below low-leakage transistor of advanced nodes (<10pA/um; low duty cycle in neuromorphic computing → static leakage dominates);
4. **High uniformity** (amorphous or nano-crystaline)
5. **Speed** (stage delay <<1ns for buffering data rates of 100M-1G bit/s)
6. **Bias stability / Reliability**
7. **Complementary** (n and p-type)
8. **Mask count** (max 1-2 additional mask per BEOL layer)
9. **Maturity** of process technology

THIN FILM TRANSISTOR (1)



THIN FILM TRANSISTOR (2)

TFT	Amorphous Si	Polysilicon	Chalcogenide (e.g. WSe_2)	Metaloxide (e.g. IGZO)	Organic (e.g. DNTT)	1D/2D (CNT, MoS, Graphene)
Mobility [cm2/Vs]	0.5-1	50-150	140	10-20	0.5-5	>100
Bias stability	very poor	good	n.a.	medium	medium	n.a.
Uniformity	good	poor	n.a.	good	good	n.a.
polarity	n	n, p	n, p	n	n, p	n, p
Ioff [A/um] @V_{GS} -10V	10p	10p *	Bad, mostly	<<1f	<10p	Very bad
Maturity	Production display	Production display	R&D Lab	Production display	R&D; Pilot line	R&D Lab
Substrate size	max. Gen10	max. Gen6	Flakes of mm^2	max. Gen8	max. Gen3.5	Wafer
Deposition process	PECVD	PECVD + anneal (laser, thermal)	Crystal growth + transfer	PVD, (solution coating)	OMBE, solution coating	CVD, transfer
Process Temperature [°C]	350	450	Growth > 600C Transfer = RT	350	150	Growth > 600C Transfer = RT

Lets look at mature TFT technologies

AMORPHOUS SILICON TFT

LCD TV – TFT IS USED AS A SWITCH IN AN ACTIVE MATRIX

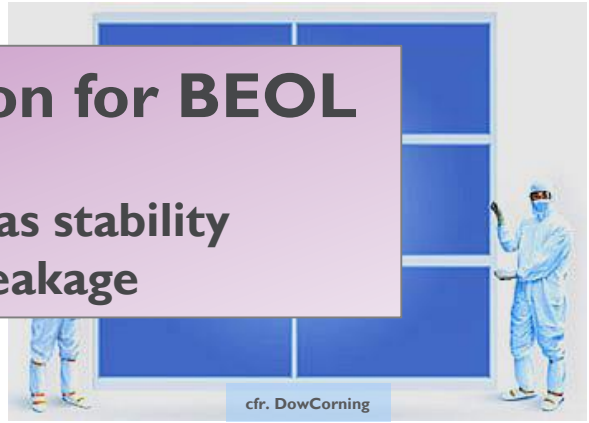
- **N-type only**
- **Low speed (mobility <1cm²/Vs)**
- **low bias stability**
- **high uniformity**
- **Temperature budget of 350°C**

No solution for BEOL

→ **too slow**

→ **too low bias stability**

→ **too high leakage**

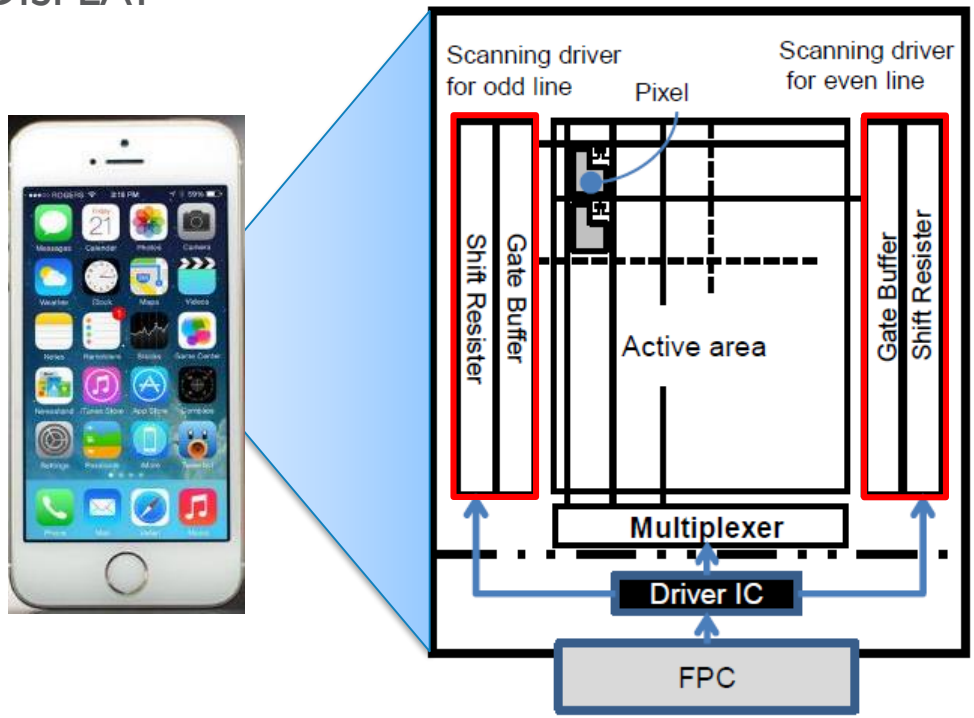


72,000 substrates per month
Investment:~ $4.25B

- Lithographically patterned amorphous silicon transistor (L=5um, μ~0.5cm²/Vs) behind every pixel
- Backplane has 4-5 mask steps

LOW-TEMPERATURE POLYSILICON TFT (1)

SMART PHONE DISPLAY

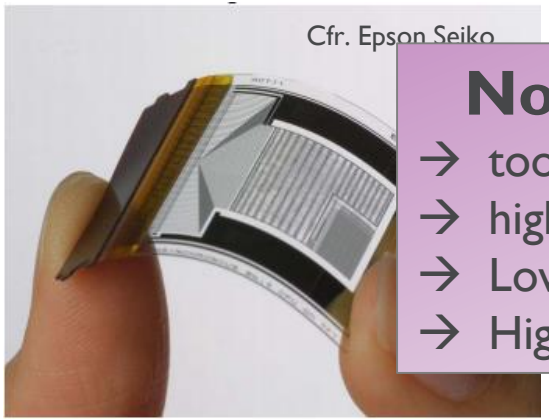


Complex in-panel digital complementary circuits with TFT

Japan Display Inc. SID DIGEST 75, 2014

LOW-TEMPERATURE POLYSILICON TFT (2)

MICROPROCESSOR



No solution for BEOL

- → too high temperature (>450°C)
- → high Ioff (grain boundaries)
- → Low uniformity (micro-crystalline)
- → High mask count (contact doping)

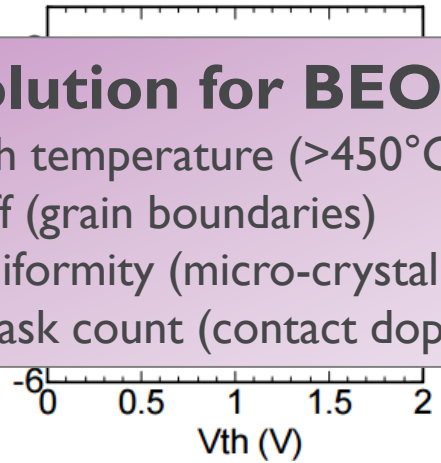


Table 1: ACT11 Specifications

Technology	LTPS TFT CMOS 2 metal layers Transistor size (Typical L/W): 4μm/12μm (N-ch) 4μm/36μm (P-ch)
Elements	~32,000 transistors
CPU Architecture	608 instructions incl. MLT & DIV 16MByte addressing space Bus release for bus masters outside 4 interrupt sources Synchronous bus interface Datapath: Bundle data, single rail
Supply Voltage	3.5-7V
Clock	30KHz-500KHz
Dimensions	27.0mm x 24.0mm x 0.2mm (Core: 12.5mm x 12.5mm x 0.2mm)
Weight	140mg (+100mg FPC)
I/O Pins	80 pins

Nobuo Karaki et al, A Flexible 8-bit Asynchronous Microprocessor Based on Low-Temperature Poly-Silicon (LTPS) TFT Technology , Digest of SID 2005, pp.1430-1433

METALOXIDE TFT

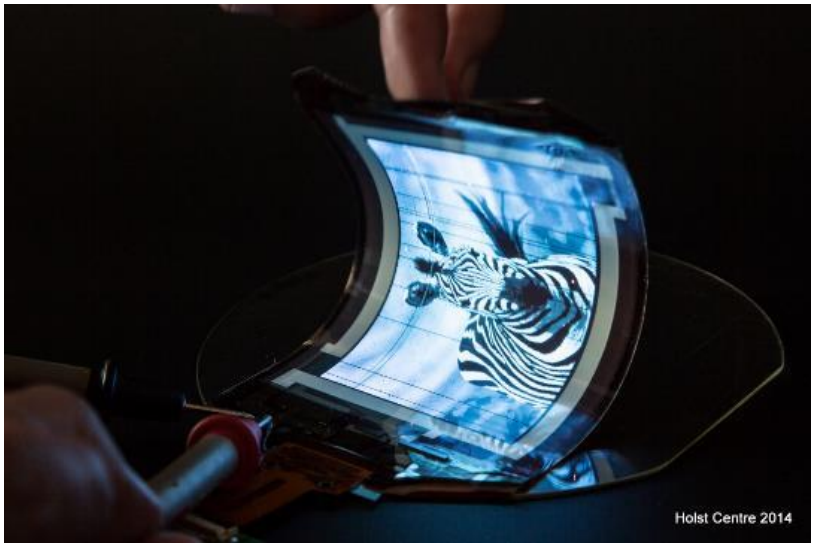
MANUFACTURING RAMP UP OF IGZO DISPLAYS SINCE 2014

Figure 8. 65-inch 4edge-Borderless UHD OLED Display

n-type only
medium speed, medium bias stability
High uniformity, ultralow Ioff
Temperature budget of 350°C

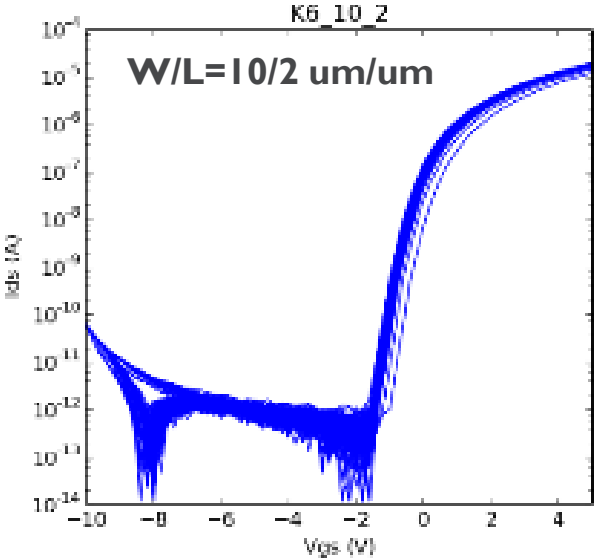
METALOXIDE TFT

FLEXIBLE AMOLED DISPLAYS @IMEC



Uniformity of IGZO TFT

(baseline PVD but ALD, CVD, Sol-gel possible)



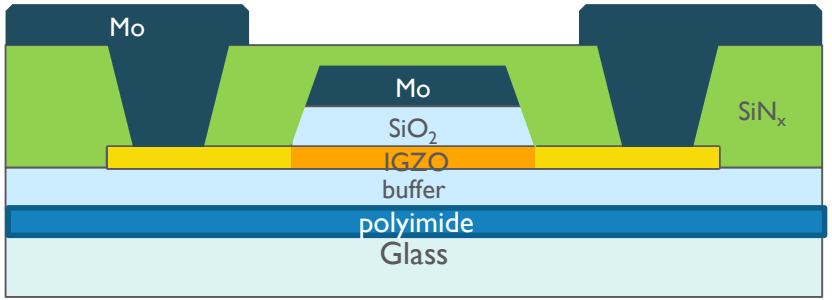
256 TFT across 6" wafer for VDD=5V technology

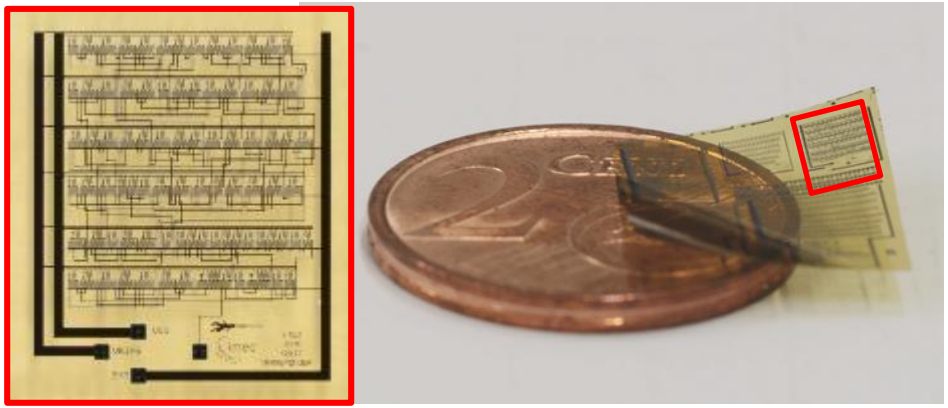
Mobility ~10cm²/Vs

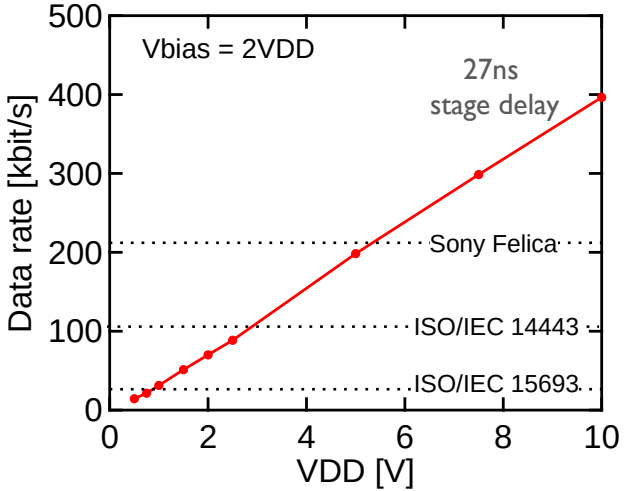
Stage delay <10ns for L=2um

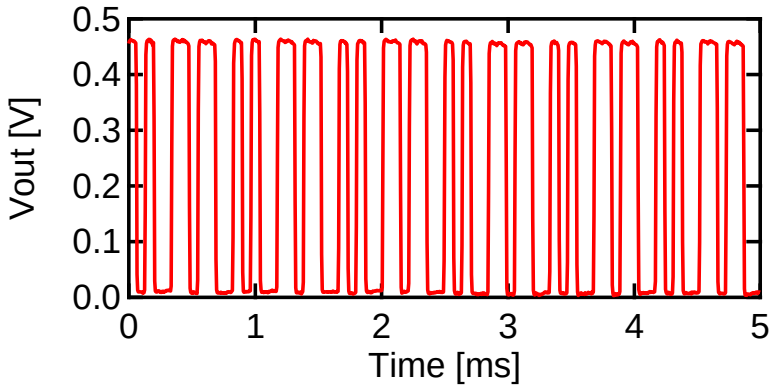
METALOXIDE TFT

RFID CHIPS WITH IGZO TFT @ IMEC









K. Myny and S.Steudel, ISSCC 2016

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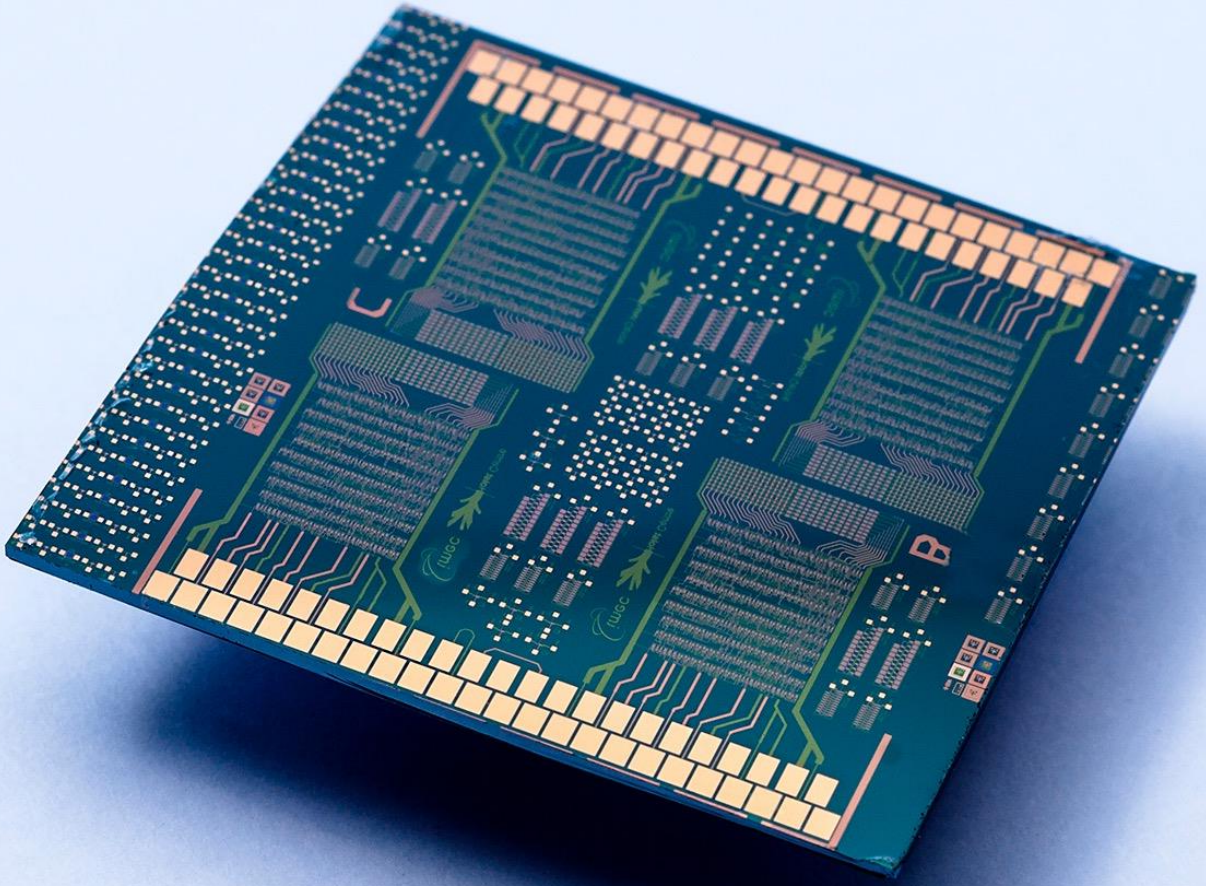
METALOXIDE TFT *THIN-FILM MICROPROCESSORS*



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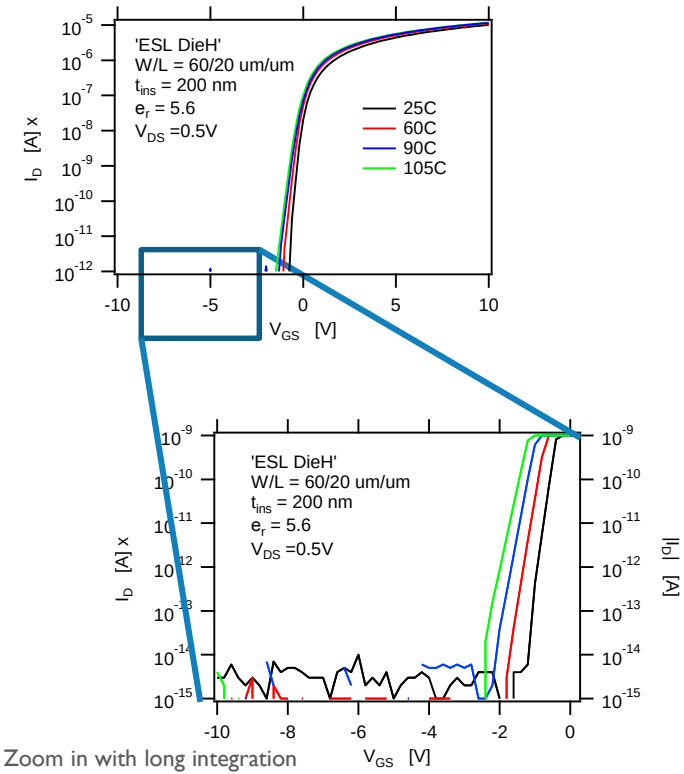
nature SCIENTIFIC REPORTS ISSCC

METALOXIDE TFT

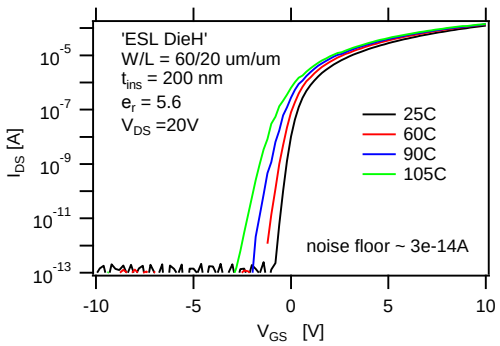
Ioff of IGZO TFT technology @ imec → wide bandgap 3.2eV without minority carriers

linear



Zoom in with long integration and auto range

saturation



Up to 105°C, the Ioff below 10^{-14}A/um. For more accurate measurement, TFT with larger W/L are required.

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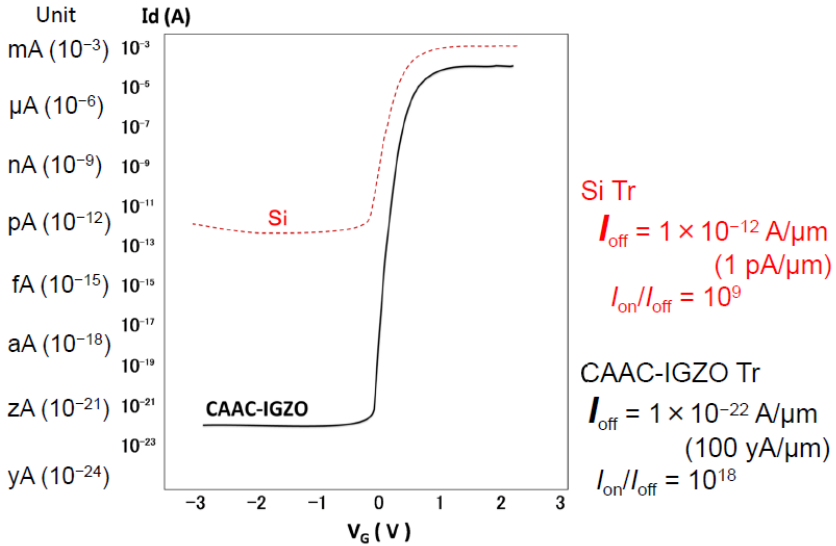
LEAKAGE CURRENT OF IGZO TFT



Si Tr

I_{off} = 1 × 10^{-12} A/μm (1 pA/μm)

I_{on}/I_{off} = 10^{9}

CAAC-IGZO Tr

I_{off} = 1 × 10^{-22} A/μm (100 yA/μm)

I_{on}/I_{off} = 10^{18}

I–V characteristics of CAAC-IGZO and Si transistors

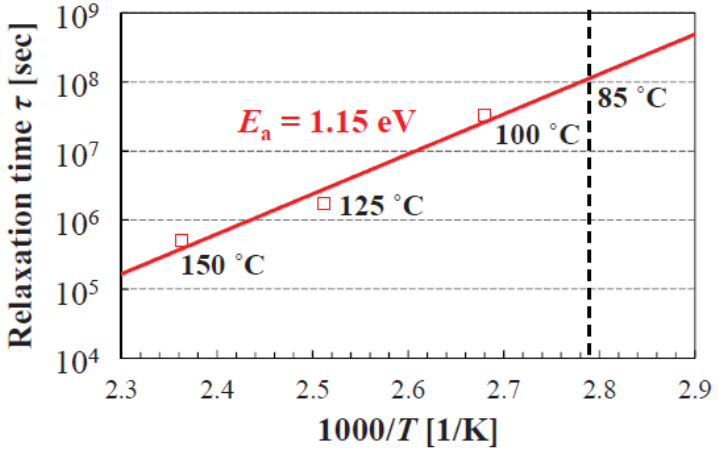


Fig. 14 Arrhenius plot of the relaxation time τ of the memory using a TGSA CAAC-IGZO FET. Activation energy E_a was estimated as 1.15 eV.

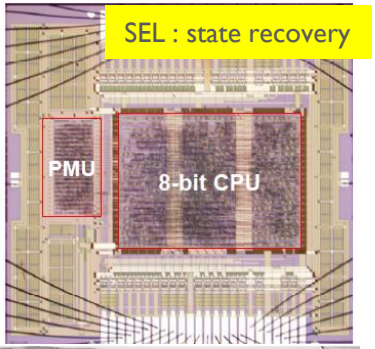
Lowest leakage current of any know material system

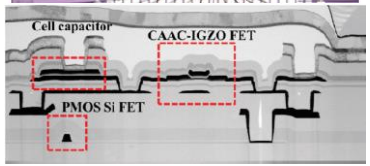
Shunpei Yamazaki, SEL (2015)

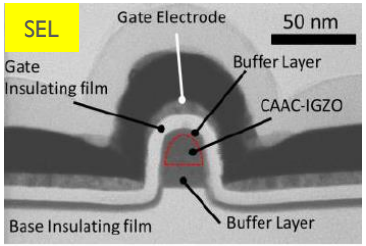
Matsubayashi et al, "20-nm-node trench-gate-self-aligned crystalline In-Ga-Zn-Oxide FET with high" IEEE IEDM, pp-141-143 (2015)

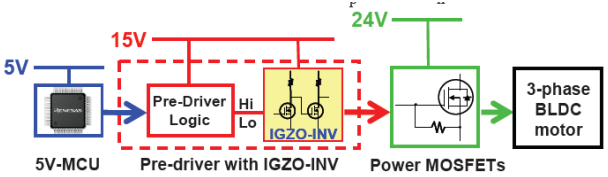
METALOXIDE TFT

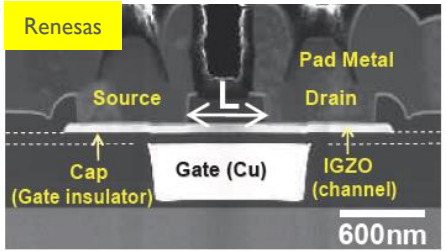
SUB-MICROMETER IGZO TFT ON CMOS

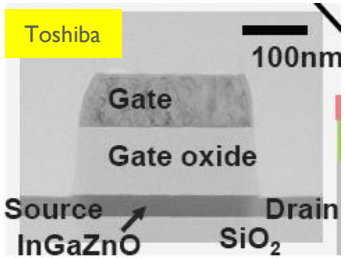


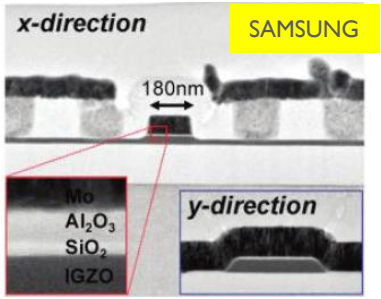


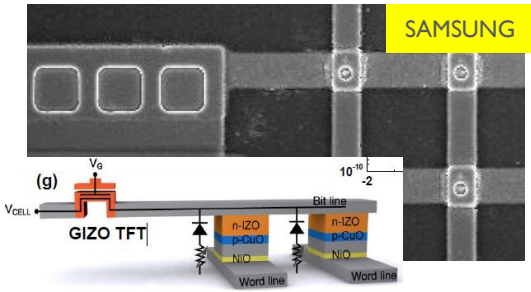












Many companies and R&D center work on metaloxide BEOL TFT for different application

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SCALABILITY OF IGZO TFT

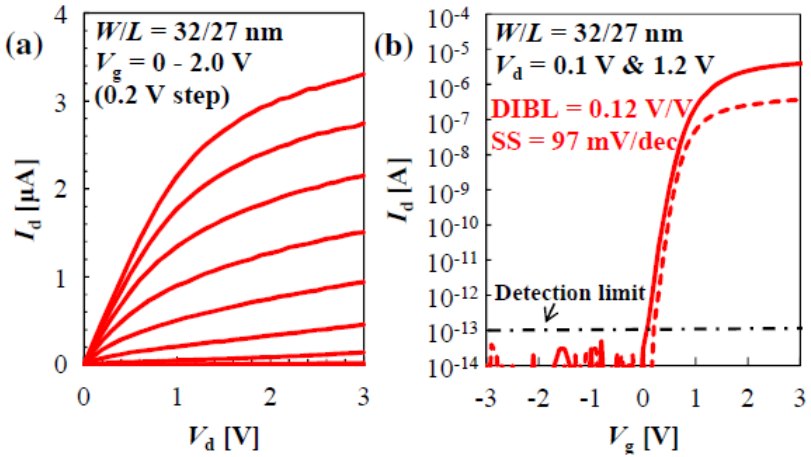


Fig. 5 (a) Output (I_d–V_d) characteristics, and (b) transfer (I_d–V_g) characteristics of a TGSA FET with W/L = 32/27 nm.

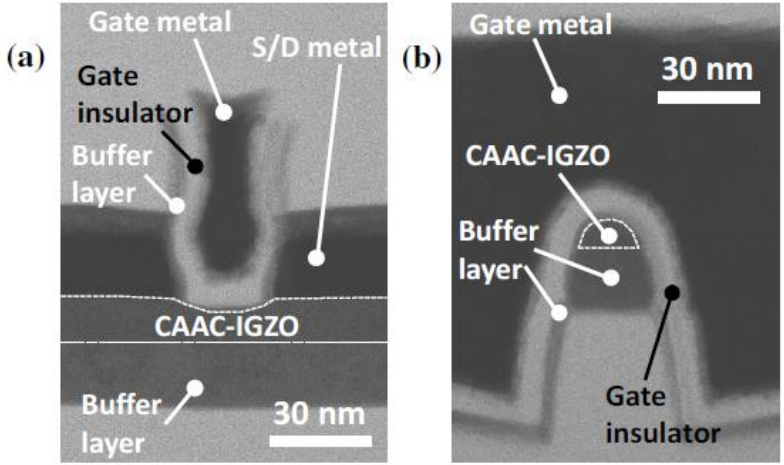


Fig. 3 Cross-sectional STEM images in the channel length direction (a) and in the channel width direction of the TGSA CAAC-IGZO FETs (b).

Matsubayashi et al, "20-nm-node trench-gate-self-aligned crystalline In-Ga-Zn-Oxide FET with high" IEEE IEDM, pp-141-143 (2015)

METALOXIDE TFT

SPEED OF SCALED IGZO TFT

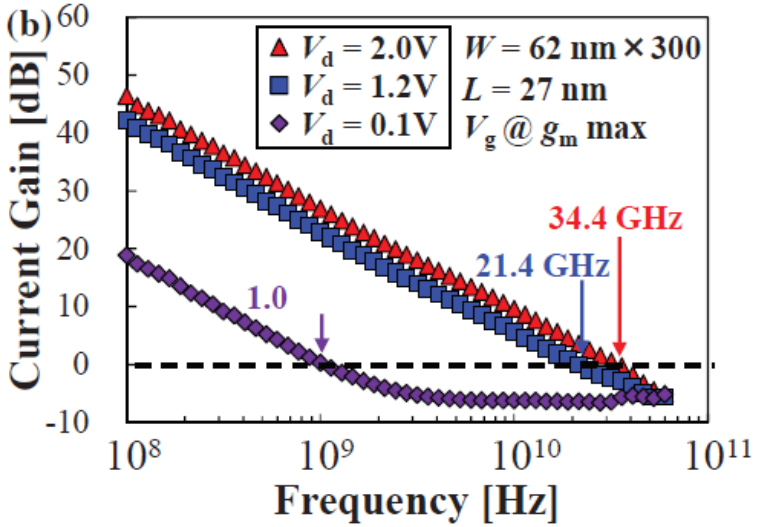


Fig. 11 (a) Transconductance g_m and (b) current gain of a TGSA CAAC-IGZO FET with 300 W/L = 62/27 nm channels connected in parallel.

IGZO has an average mobility ~ 10cm²/Vs. Higher mobility metaloxide material with mobility >40cm²/Vs have been demonstrated

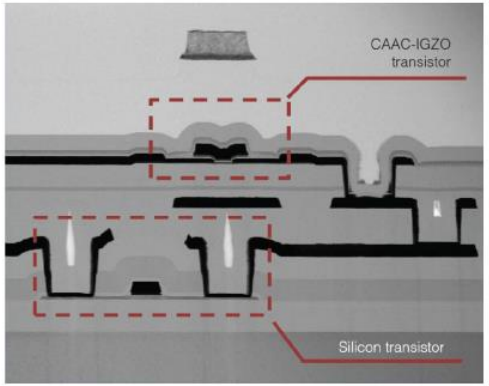
Matsubayashi et al, "20-nm-node trench-gate-self-aligned crystalline In-Ga-Zn-Oxide FET with high" IEEE IEDM, pp-141-143 (2015)

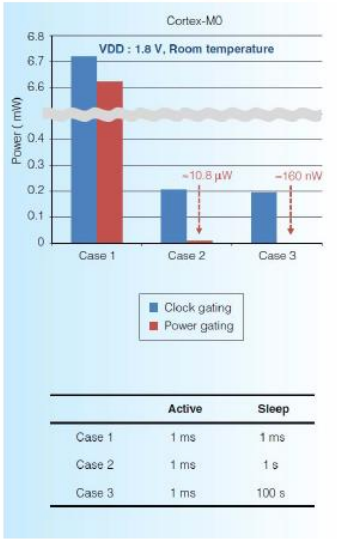
METALOXIDE TFT

VLSI INTEGRATION ON CMOS

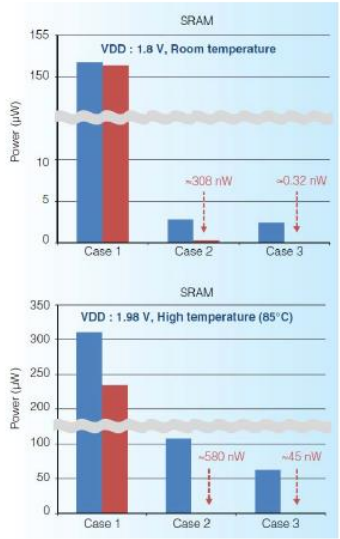
EMBEDDED SRAM AND CORTEX-M0 CORE USING A 60-NM CRYSTALLINE OXIDE SEMICONDUCTOR

Semiconductor Energy Laboratory
University of Tokyo
ARM Nokia





	Active	Sleep
Case 1	1 ms	1 ms
Case 2	1 ms	1 s
Case 3	1 ms	100 s



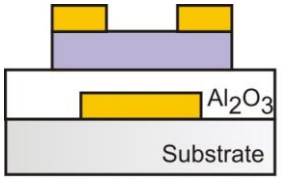
H. Tamura *et al.*, IEEE. Micro, vol.**34**, no.6, pp.42-53, Nov./Dec. 2014

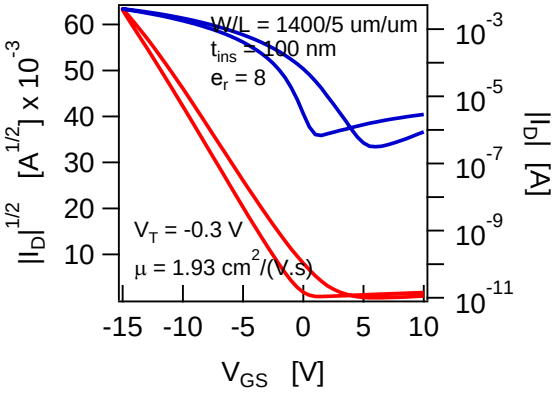
IGZO TFT LOOKS LIKE THE PERFECT BEOL TFT SOLUTION BUT.....

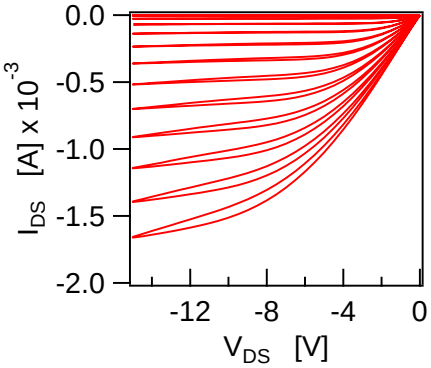
METALOXIDE TFT

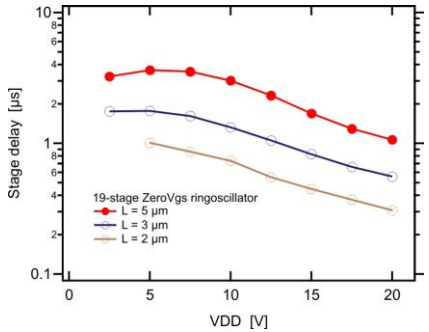
P-TYPE TFT

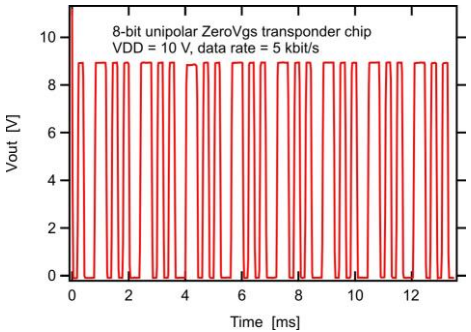
SnOx at 350 °C











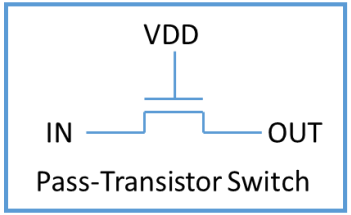
Lower mobility <5cm²/Vs
High Ioff >1nA/um
Low bias stability
Low maturity

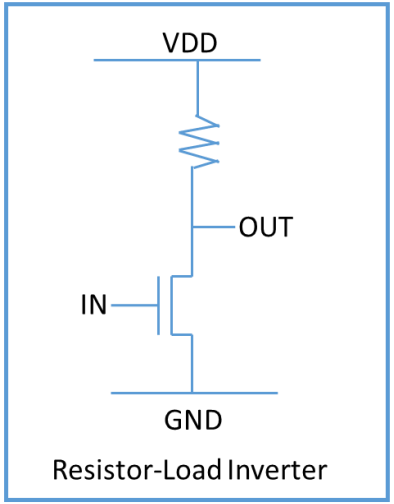
Ab-initio modeling suggest that an amorphous metaloxide TFT with better performance is unlikely

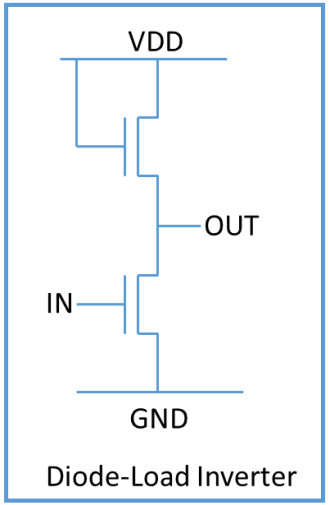
TFT CIRCUIT LOGIC / DEVICE LIMITATION !!

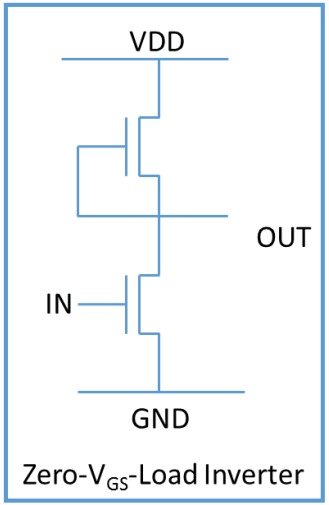
Unipolar Logic

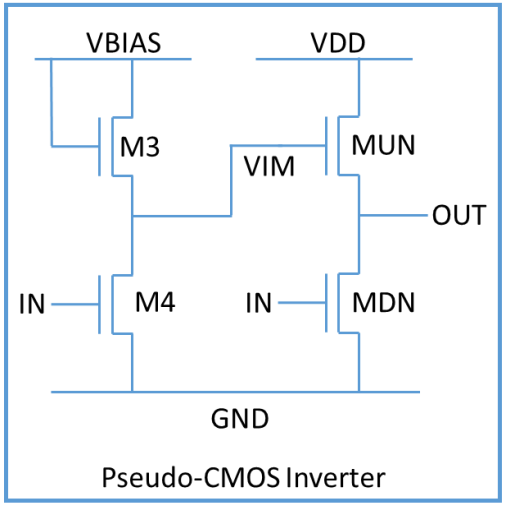
- Limited Noise Margins
- Poor Gain
- Non-symmetric VTC (Vm /= Vdd/2)
- Can be improved using higher Vdd and thinner gate dielectric











3D BEOL TFT FOR GLOBAL SYNAPSE

METALOXIDE TFT

1. **Scalability** down to pitch of M3-M4 (L<50nm)
2. **Temperature** budget of BEOL (380°C)
3. **Leakage** below low-leakage transistor of advanced nodes (<10pA/um)
4. **High uniformity** (amorphous or nano-crystaline)
5. **Speed** (stage delay <<1ns for buffering data rates of 1Gbit/s)
6. **Bias stability / reliability**
7. **Complementary** (n and p-type)
8. **Cost** (max 1-2 additional mask per BEOL layer)
9. **Maturity** of process technology on CMOS

Will this approach translate into lower energy consumption, smaller footprint and lower cost then conventional FEOL solutions for global synapse reconfigurable interconnect?

H2020: NEU-RAM3

BEOL TFT TEST CHIP WITH RECONFIGURABLE INTERCONNECT (3000-4000 TFT)

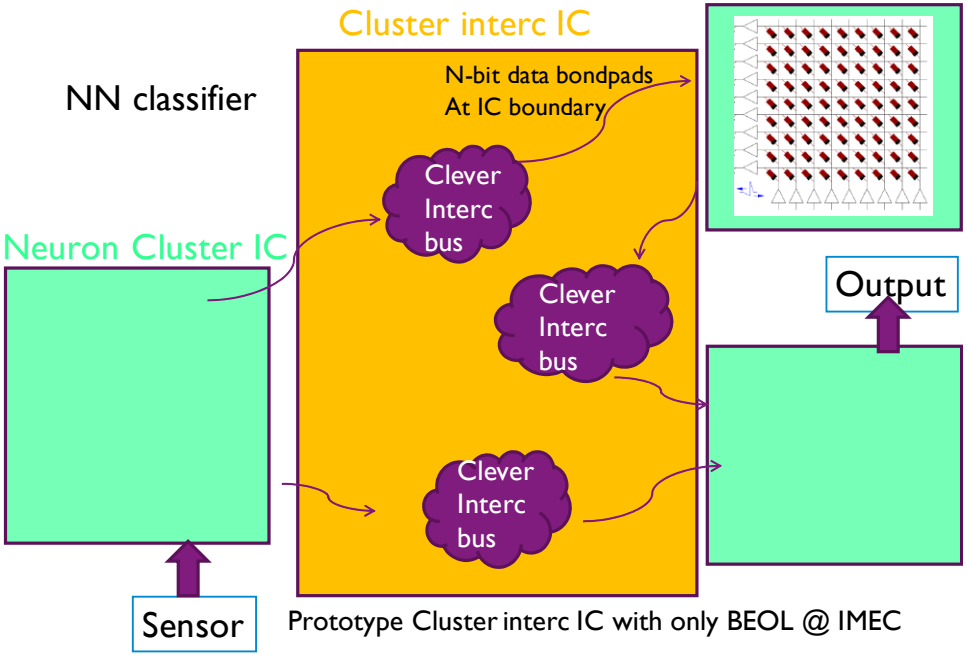


Figure 10: conceptual implementation with several neural clusters ICs with central scalable global synapse communication IC.